UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,868	12/10/2003	Han-Gu Sohn	8729-226 (ID-200306-011-1	6860

22150 7590 01/18/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
DARE, RYAN A	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/732,868	SOHN ET AL.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/03, 12/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 09/22/05*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 10-15, 20-21, and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanabe, US Patent 6,052,330.

3. With respect to claim 1, Tanabe teaches a semiconductor memory device comprising:

a memory cell array, in fig. 1, MEM.

a data buffer for processing data read from or written to the memory cell array, in fig. 1, data control part 3; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal, in fig. 1, control part 5.

Although Tanabe does not explicitly call the data control part 3 a data buffer, it is apparent from the detailed description of the data control circuits 9 that the data control part 3 buffers the data for inputs and outputs. Referring to fig. 3, the data control circuit 9 contains flip flops FF3 through FF10 that buffer data for input and output. This is generally discussed in col. 3, line 34 through col. 4 line 42.

Control part 5 functions as a data width control circuit because it contains the data mask control circuit 7, and sends control signals DOUTM, DINM1, and DINM2 to data control part 3, which control which bits are masked, and therefore how many bits are input/output to the memory (i.e. the data width).

4. With respect to claim 2, Tanabe teaches the device of claim 1, wherein the data width control circuit comprises:

a decoder for decoding the external address signal in response to a data access command to generate a first control signal, in fig. 1, where the control part 5 takes the column address signal CASB and the row address signal RASB and controls the memory via the control signals CSM. See the related discussion in col. 2, lines 19-38; and

a data buffer controller responsive to the first control signal, to generate a second control signal for controlling the data width of the data buffer, in fig. 1, data mask control circuit 7, which in the case of an output data mask, generates the control signal DOUTM. See the related discussion in col. 2, lines 24-27.

5. With respect to claim 3, Tanabe teaches the device of claim 1, wherein the data width control circuit selectively controls the data width of the data buffer by generating a control signal that masks or unmasks one or more bits of the data buffer, in col. 2, lines 24-27.

6. With respect to claim 4, Tanabe teaches the device of claim 3, wherein a masked bit is prevented from being input to the memory cell array from the data buffer, in col. 1, lines 34-50.

7. With respect to claim 5, Tanabe teaches the device of claim 3, wherein a masked bit is prevented from being output from the data buffer, in col. 1, lines 34-50.

8. With respect to claim 6, Tanabe teaches the device of claim 1, wherein the data buffer has a width of n bits and wherein the data width of the data buffer is selectively controlled to be n bits or less, in col. 8, lines 38-41, which represents the case where no bits are masked, thereby causing the data width to be n bits, and in col. 8, lines 5-9, where some of the data bits are masked, thereby causing the data width to be less than n bits.

9. With respect to claim 10, Tanabe teaches a semiconductor memory device comprising:

a memory cell array, in fig. 1, MEM.

a data output buffer for outputting data read from the memory cell array, in fig. 1, data control part 3;

a data input buffer for inputting data to be written to the memory cell array, in fig. 1, data control part 3; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal, in fig. 1, control part 5.

Although Tanabe does not explicitly call the data control part 3 a data buffer, it is apparent from the detailed description of the data control circuits 9 that the data control part 3 buffers the data for inputs and outputs. Referring to fig. 3, the data control circuit

9 contains flip flops FF3 through FF10 that buffer data for input and output. This is generally discussed in col. 3, line 34 through col. 4 line 42.

Control part 5 functions as a data width control circuit because it contains the data mask control circuit 7, and sends control signals DOUTM, DINM1, and DINM2 to data control part 3, which control which bits are masked, and therefore how many bits are input/output to the memory (i.e. the data width).

10. With respect to claim 11, Tanabe teaches the device of claim 10, wherein the data width control circuit comprises:

a decoder which is activated in response to a read command signal or write command signal to decode the external address to generate a first control signal, in fig. 1, where the control part 5 takes the column address signal CASB and the row address signal RASB and controls the memory via the control signals CSM. See the related discussion in col. 2, lines 19-38; and

a data input buffer controller responsive to the first control signal, to generate a second control signal for controlling the data width of the data buffer, in fig. 1, data mask control circuit 7, which in the case of an input data mask, generates the control signals DINM1 and DINM2.

a data output buffer controller responsive to the first control signal, to generate a second control signal for controlling the data width of the data buffer, in fig. 1, data mask control circuit 7, which in the case of an output data mask, generates the control signal DOUTM. See the related discussion in col. 2, lines 24-27.

11. With respect to claim 12, Tanabe teaches the device of claim 10, wherein the data width control circuit selectively controls the data width of the data input buffer or data output buffer by generating a control signal that masks or unmasks one or more bits of the data buffer, in col. 2, lines 24-27.

12. With respect to claim 13, Tanabe teaches the device of claim 12, wherein a masked bit is prevented from being input to the memory cell array from the data buffer, in col. 1, lines 34-50.

13. With respect to claim 14, Tanabe teaches the device of claim 12, wherein a masked bit is prevented from being output from the data buffer, in col. 1, lines 34-50.

14. With respect to claim 15, Tanabe teaches the device of claim 10, wherein the data input and output buffers has a width of n bits and wherein the data width of the data buffer is selectively controlled to be n bits or less, in col. 8, lines 38-41, which represents the case where no bits are masked, thereby causing the data width to be n bits, and in col. 8, lines 5-9, where some of the data bits are masked, thereby causing the data width to be less than n bits.

15. With respect to claim 20, Tanabe teaches an integrated circuit device, comprising:

a data buffer, in fig. 1, data control part 3; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal, in fig. 1, control part 5.

Although Tanabe does not explicitly call the data control part 3 a data buffer, it is apparent from the detailed description of the data control circuits 9 that the data control part 3 buffers the data for inputs and outputs. Referring to fig. 3, the data control circuit 9 contains flip flops FF3 through FF10 that buffer data for input and output. This is generally discussed in col. 3, line 34 through col. 4 line 42.

Control part 5 functions as a data width control circuit because it contains the data mask control circuit 7, and sends control signals DOUTM, DINM1, and DINM2 to data control part 3, which control which bits are masked, and therefore how many bits are input/output to the memory (i.e. the data width).

16. With respect to claim 21, Tanabe teaches a memory system, comprising:

a controller for generating data access command signals and address signals, in fig. 1 where the controller is providing the signals RASB, CASB, WEB, DQM1, DQM2, CLOCK, and AB; and

a semiconductor memory device comprising:

a memory cell array, in fig. 1, MEM.

a data buffer for processing data read from or written to the memory cell array, in fig. 1, data control part 3; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal, in fig. 1, control part 5.

Although Tanabe does not explicitly call the data control part 3 a data buffer, it is apparent from the detailed description of the data control circuits 9 that the data control

part 3 buffers the data for inputs and outputs. Referring to fig. 3, the data control circuit 9 contains flip flops FF3 through FF10 that buffer data for input and output. This is generally discussed in col. 3, line 34 through col. 4 line 42.

Control part 5 functions as a data width control circuit because it contains the data mask control circuit 7, and sends control signals DOUTM, DINM1, and DINM2 to data control part 3, which control which bits are masked, and therefore how many bits are input/output to the memory (i.e. the data width).

17. With respect to claim 25, Tanabe teaches a method for providing data I/O (input/output) width control in a semiconductor memory device, comprising the steps of:

generating a data width control signal in response to an external address signal, in fig. 1, control part 5; and

controlling a data width of a data buffer in response to the data width control signal, in col. 2, lines 24-27.

18. With respect to claim 26, Tanabe teaches a semiconductor memory device, comprising:

a memory cell array, in fig. 1, MEM;

a data buffer for processing data read from or written to the memory cell array by a read command or write command, in fig. 1, data control part 3; and

a data width control circuit for selectively controlling a data width of the data buffer in response to an external address signal accompanied with the read command or write command, in fig. 1, control part 5.

19. With respect to claim 27, Tanabe teaches a semiconductor memory device, comprising:

a memory cell array, in fig. 1, MEM;

a data buffer for processing data read from or written to the memory cell array by a read command or write command, in fig. 1, data control part 3; and

a data width control circuit for selectively controlling a data width of the data buffer in response to a redundant external address signal accompanied with the read command or write command, in fig. 1, control part 5.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

22. Claims 7-9 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe as applied to claims 1-6, 10-15, 20-21, and 25-27 above, in view of Miyata et al., US Patent 4,706,219.

23. With respect to claim 7, Tanabe teaches all other limitations of the parent claims as discussed supra, but fails to teach a decoder as described by claim 7. Miyata et al. teach a decoder which comprises:

a switching circuit, in fig. 7, switch 1; and

a logic circuit, wherein the switching circuit is response to the data access command to pass the external address signal to the logic circuit and wherein the logic circuit processes the external command to generate the first control signal based on the external command, in fig. 7 and col. 5 lines 60-65.

24. With respect to claim 8, the combination of Tanabe and Miyata et al. teach all other limitations of the parent claims as discussed supra. In addition, Miyata et al. teach the device of claim 7, wherein the logic circuit comprises a plurality of parallel connected AND gates that receive the external address signal, and wherein the first control signal comprises a plural bit signal comprised of the output signals from the AND gates, in col. 6, lines 15-19.

25. With respect to claim 9, the combination of Tanabe and Miyata et al. teach all other limitations of the parent claims as discussed supra. In addition, Tanabe teaches the device of claim 8, wherein the data buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the data access command, and wherein one or more switches are

selectively activated in response to the first control signal to generate the second control signal, the second control signal comprise a plural bit signal comprised of the output signals of the switches, in fig. 2, where FF1 and FF2 are the switches, and the output signal is DOUTM.

26. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the variable data length storage memory of Tanabe with the variable data length storage memory of Miyata et al. The patent issued to Tanabe does not go into the structural detail necessary to read on independent claims 7-9, although the function is very similar. The patent issued to Miyata et al. does go into sufficient detail about the underlying implementation to enable the reference of Tanabe to perform the functions necessary, such as generating the control signals to control the memory.

27. With respect to claim 16, Tanabe teaches all other limitations of the parent claims as discussed supra, but fails to teach a decoder as described by claim 7. Miyata et al. teach a decoder which comprises:

a switching circuit, in fig. 7, switch 1; and

a logic circuit, wherein the switching circuit is response to the data access command to pass the external address signal to the logic circuit and wherein the logic circuit processes the external command to generate the first control signal based on the external command, in fig. 7 and col. 5 lines 60-65.

28. With respect to claim 17, the combination of Tanabe and Miyata et al. teach all other limitations of the parent claims as discussed supra. In addition, Miyata et al. teach

the device of claim 7, wherein the logic circuit comprises a plurality of parallel connected AND gates that receive the external address signal, and wherein the first control signal comprises a plural bit signal comprised of the output signals from the AND gates, in col. 6, lines 15-19.

29. With respect to claim 18, the combination of Tanabe and Miyata et al. teach all other limitations of the parent claims as discussed supra. In addition, Tanabe teaches the device of claim 8, wherein the data buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the write command signal, and wherein one or more switches are selectively activated in response to the first control signal to generate the second control signal, the second control signal comprise a plural bit signal comprised of the output signals of the switches, in fig. 2, where FF1 and FF2 are the switches, and the output signal is DOUTM.

30. With respect to claim 19, the combination of Tanabe and Miyata et al. teach all other limitations of the parent claims as discussed supra. In addition, Tanabe teaches the device of claim 8, wherein the data buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the read command signal, and wherein one or more switches are selectively activated in response to the first control signal to generate the second control signal, the second control signal comprise a plural bit signal comprised of the output signals of the switches, in fig. 2, where FF1 and FF2 are the switches, and the output signal is DOUTM.

31. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the variable data length storage memory of Tanabe with the variable data length storage memory of Miyata et al. The patent issued to Tanabe does not go into the structural detail necessary to read on independent claims 7-9, although the function is very similar. The patent issued to Miyata et al. does go into sufficient detail about the underlying implementation to enable the reference of Tanabe to perform the functions necessary, such as generating the control signals to control the memory.

32. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanabe as applied to claims 1-6, 10-15, 20-21, and 25-27 above, in view of Hirai, US Patent 5,349,448.

33. With respect to claim 22, Tanabe teaches all limitations of the parent claims, but fails to explicitly describe that the controller is a microprocessor unit. Hirai teaches that the controller for use in the present invention can be a microprocessor unit, in col. 1, lines 32-35.

34. It would be obvious to one of ordinary skill in the art to modify the invention of Tanabe with the invention of Hirai to use a microprocessor unit as a controller in a storage system, because microprocessors are extremely well known in the art as ways to implement a controller.

35. With respect to claim 23, Tanabe teaches all limitations of the parent claims, but fails to explicitly describe that the controller is a network control unit. Hirai teaches that

the controller for use in the present invention can be a network control unit, in col. 1, lines 40-41.

36. It would be obvious to one of ordinary skill in the art to modify the invention of Tanabe with the invention of Hirai to use a network control unit as a controller in a storage system, because in the case where the invention is implemented over a network, a network control unit is necessary as in the system of Hirai.

37. With respect to claim 24, Tanabe teaches all limitations of the parent claims, but fails to explicitly describe that the controller is a memory controller. Hirai teaches that the controller for use in the present invention can be a memory controller, in col. 1, lines 32-35 and fig.1, where it is obvious that the controller controls image memory and is therefore a memory controller.

38. It would be obvious to one of ordinary skill in the art to modify the invention of Tanabe with the invention of Hirai to use a memory controller as a controller in a storage system, because when you have a controller that controls memory, as is the case in the present invention, Tanabe, and in Hirai, the controller is a memory controller.

Conclusion

39. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory systems.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
January 11, 2006

MATTHEW D. ANDERSON
PRIMARY EXAMINER